

PATENT
Reply under 37 CFR 1.116
EXPEDITED PROCEDURE
Group 2121

AMENDMENTS TO THE CLAIMS

1. (currently amended) A method of regulating a target system, comprising the steps of:
- providing a reference signal;
- generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;
- 5 providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;
- comparing said frequency of said reference pulse train with said frequency of said feedback pulse train and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;
- 10 generating a control signal dependent upon said comparison without regard to phase locking said feedback pulse train to said reference signal; and
- providing said control signal as an input to said target system.
2. (cancelled)
3. (currently amended) The method of regulating a target system of claim 1 2, wherein said step of generating said control signal comprises the substep of generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said
- 5 feedback pulse train.

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4. (previously presented) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

5 providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

substantially aligning a leading edge of each digital signal in said reference pulse train
10 with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison without regard to phase locking said feedback pulse train to said reference signal, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital
15 signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first proportional clock CP1 at a frequency FP1 when said digital signals of said proportional error pulse train are in a high state;

20 resetting said first proportional clock CP1 to zero when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first proportional clock CP1 into a second proportional clock CP2 each time said first proportional clock CP1 transitions

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from a high state to a low state;

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counting down from said loaded current value with said second
proportional clock CP2 at a frequency f_{P2} until a zero value is reached; and

determining a proportional error term representing a time average of a
signal which is held high while said second proportional clock CP2 is in a high
state and held low while said second proportional clock CP2 is in a zero state, said

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control signal being dependent upon said proportional error term; and
providing said control signal as an input to said target system.

5. (original) The method of regulating a target system of claim 3, wherein said step of
generating said control signal comprises the further substep of generating an error direction pulse
train including a plurality of digital signals, each said digital signal representing a directionality of
said error between said corresponding pair of aligned digital signals.

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6. (previously presented) A method of regulating a target system, comprising the steps of:
providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency
dependent upon said reference signal;

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providing a target system to be regulated, said target system having an output in the form
of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said
feedback pulse train, and substantially aligning a leading edge of each digital signal in said
reference pulse train with a leading edge of each digital signal in said feedback pulse train;

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10 generating a control signal dependent upon said comparison without regard to phase
locking said feedback pulse train to said reference signal, said generating step including the
substeps of:

15 generating a proportional error pulse train including a plurality of digital
signals, each said digital signal representing an error between a corresponding pair
of aligned digital signals of said reference pulse train and said feedback pulse train;

 generating an error direction pulse train including a plurality of digital
signals, each said digital signal representing a directionality of said error between
said corresponding pair of aligned digital signals;

20 counting up from zero with a first integral clock CI1 at a frequency fI1
when said digital signals of said proportional error pulse train are in a high state
and said digital signals of said error direction pulse train are simultaneously in a
high state;

25 counting down with said first integral clock CI1 at said frequency fI1 when
said digital signals of said proportional error pulse train are in a high state and said
digital signals of said error direction pulse train are in a low state;

 maintaining said first integral clock CI1 at a current value when said digital
signals of said proportional error pulse train are in a low state;

30 loading a current value of said first integral clock CI1 into a second integral
clock CI2 each time said first integral clock CI1 transitions from a high state to a
low state;

 counting down from said loaded current value with said second integral
clock CI2 at a frequency fI2 until a zero value is reached; and

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determining an integral error term representing a time average of a signal
which is held high while said second integral clock CI2 is in a high state and held
35 low while said second integral clock CI2 is in a zero state, said control signal being
dependent upon said integral error term; and
providing said control signal as an input to said target system.

7. (previously presented) A method of regulating a target system, comprising the steps of:
providing a reference signal;
generating a plurality of digital signals defining a reference pulse train with a frequency
dependent upon said reference signal;
5 providing a target system to be regulated, said target system having an output in the form
of a plurality of digital signals defining a feedback pulse train having a frequency;
comparing said frequency of said reference pulse train with said frequency of said
feedback pulse train, and substantially aligning a leading edge of each digital signal in said
reference pulse train with a leading edge of each digital signal in said feedback pulse train;
10 generating a control signal dependent upon said comparison without regard to phase
locking said feedback pulse train to said reference signal, said generating step including the
substeps of:
generating a proportional error pulse train including a plurality of digital
signals, each said digital signal representing an error between a corresponding pair
15 of aligned digital signals of said reference pulse train and said feedback pulse train;
counting up from zero with a first derivative clock CD1 at a frequency $fD1$
when said digital signals of said proportional error pulse train are in a high state;

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20 subtracting a current state of said first derivative clock CD1 from a current
state of a register R each time said first derivative clock CD1 transitions from a
high state to a low state;
loading said subtracted state into a second derivative clock CD2;
loading said current state of said first derivative clock CD1 into said
register R;
resetting said first derivative clock CD1 to zero;
25 counting down with said second derivative clock CD2 at a frequency fD2
after said subtracted state is loaded therein;
maintaining said first integral clock CI1 at a current value when said digital
signals of said proportional error pulse train are in a low state; and
determining a derivative error term representing a time average of a signal
30 which is held high while said second derivative clock CD2 is in a high state and
held low while said second derivative clock CD2 is in a zero state, said control
signal being dependent upon said derivative error term; and
providing said control signal as an input to said target system.

8. (currently amended) The A method of regulating a target system, ~~of claim 1, wherein~~
comprising the steps of:

providing a reference signal;
generating a plurality of digital signals defining a reference pulse train with a frequency
5 dependent upon said reference signal;

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providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency, said frequency of said feedback pulse train varies varying with time;

10 comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

generating a control signal dependent upon said comparison without regard to phase locking said feedback pulse train to said reference signal; and

providing said control signal as an input to said target system.